UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,895,420 B1
APPLICATION NO. : 09/505382
DATED : May 17, 2005
INVENTOR(S) : Roy R. Faget

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS

Claim 1, Column 6, line 19, after "dual" insert --rail--

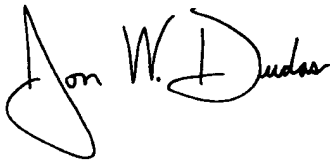
Claim 9, Column 7, line 2, delete "transistor" and insert therefor --field effect transistor (FET)--

Claim 9, Column 7, line 19, after "data transistors required" insert --wherein each of the logic gates provides complementary outputs as the shifted data output--

Claim 15, Column 8, line 16, delete "data to" and insert therefor --data from the shared data lines into--

Signed and Sealed this

Twentieth Day of May, 2008



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Director of the United States Patent and Trademark Office